

MS-7720 VER: 1.1

CPU:

AMD FT1

System Chipset:

AMD HUDSON-D1

On Board Chipset:

Super I/O -- Fintek F71889AD

LAN -- RTL8111E

HD Codec -- ALC887 co-lay 892

BIOS -- SPI ROM 4M

Main Memory:

DDR III X 2 (Max 8GB)

Expansion Slots:

PCI-E X 16 *1

PCI-E X 1 *2

PCI X 1

Clock Generator:

FCH Internal CLK GEN

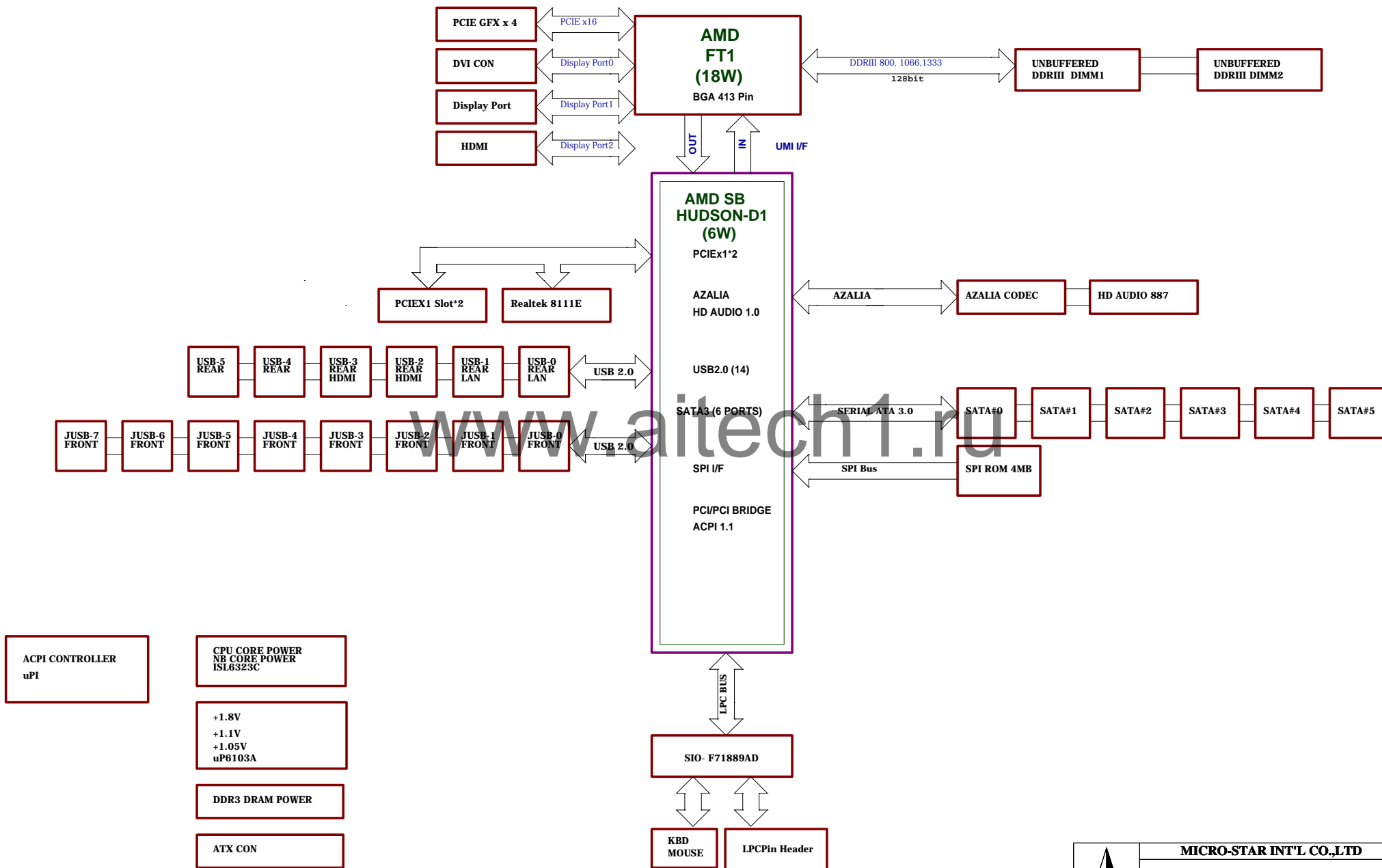
PWM:

Controller -- Intersil ISL6323C



Title	Page
Cover Sheet	1
Block Diagram	2
ISL6265C	3
CPU FT1 MEM/PCIE/UMI	4
CPU FT1 DISPLY & MISC	5
CPU FT1 PWR&GND	6
DDR DIMM1/2	7
FCH-2 PCIE/PCI/CPU/LPC/CLK	8
FCH-2 ACPI/GPIO/USB/PHY/AZ	9
FCH-2 SATA/SPI/VGA	10
FCH-2 POWER & GND	11
FCH-2 STRAPPING	12
PCI EXPRESS X16, X1 SLOT	13
PCI X1	14
HDMI	15
VGA	16
DVI	17
F71889AD	18
USB2.0 CONN	19
Audio ALC887/892	20
LAN - RTL 8111E	21
FAN	22
VCC_DDR & VTT_DDR	23
+1.8V/+1.1V/+1.0V	24
Standby power	25
ATX/Front Panel/KB/EMI	26
BOM - Option Parts	27

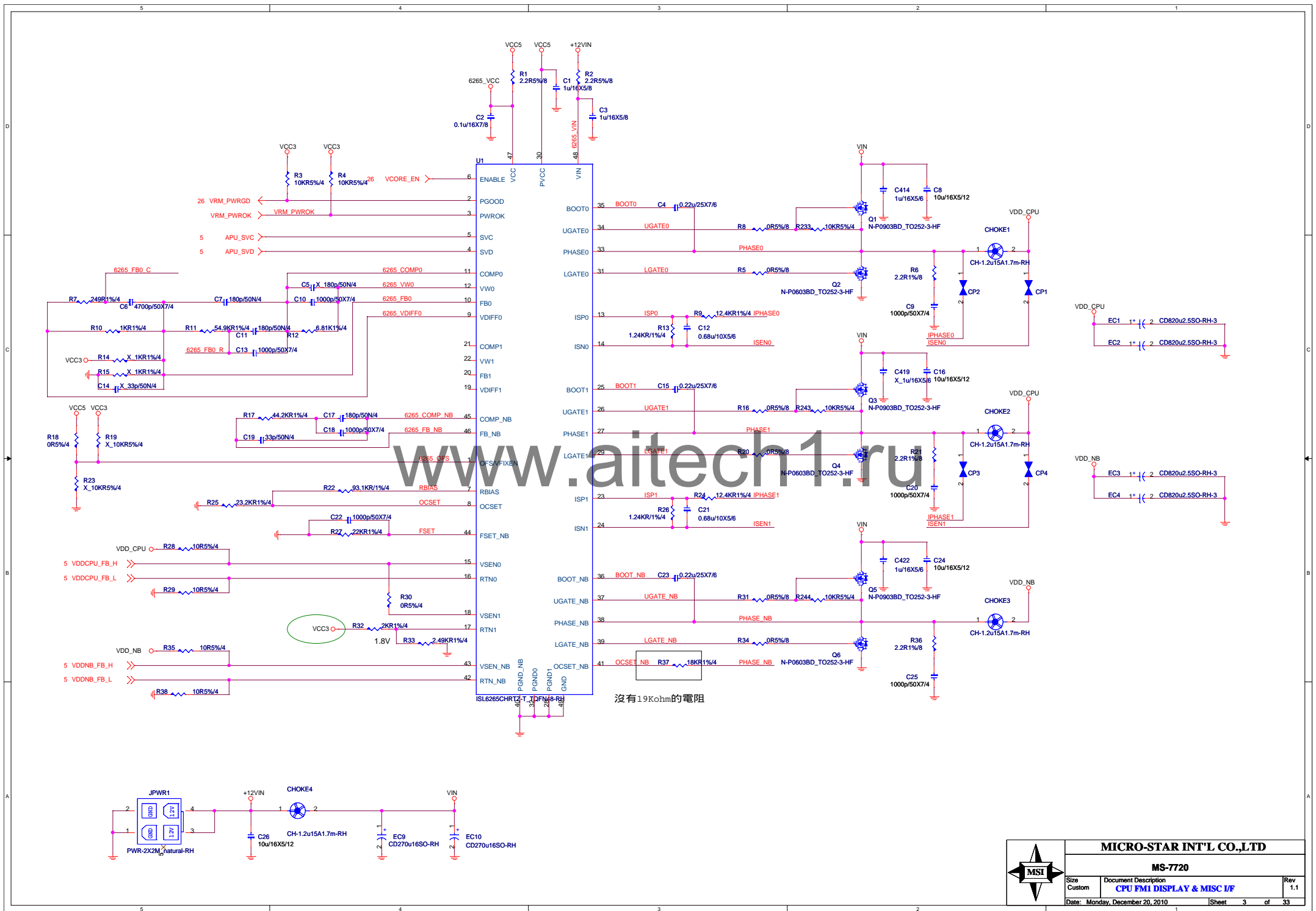
Project MS-7720 BLOCK DIAGRAM



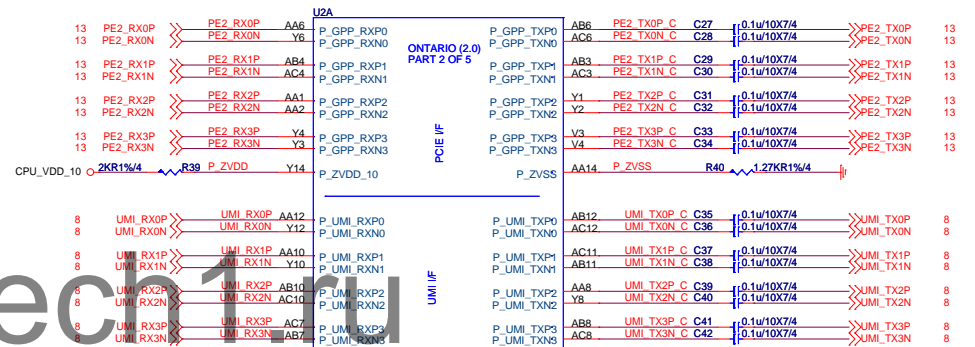
MICRO-STAR INT'L CO.,LTD

MS-7720

Size	Document Description	Rev
Custom	Block Diagram	1.1
Date: Monday, December 20, 2010		Sheet 2 of 33

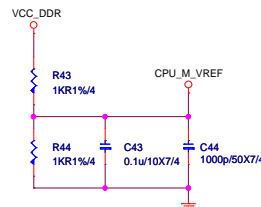


7 MEM_MA_DQS_L[7..0] << MEM_MA_DQS_L[7..0]
 7 MEM_MA_DQS_H[7..0] << MEM_MA_DQS_H[7..0]
 7 MEM_MA_DM[7..0] << MEM_MA_DM[7..0]
 7 MEM_MA_ADD[15..0] << MEM_MA_ADD[15..0]
 7 MEM_MA_DATA[63..0] << MEM_MA_DATA[63..0]

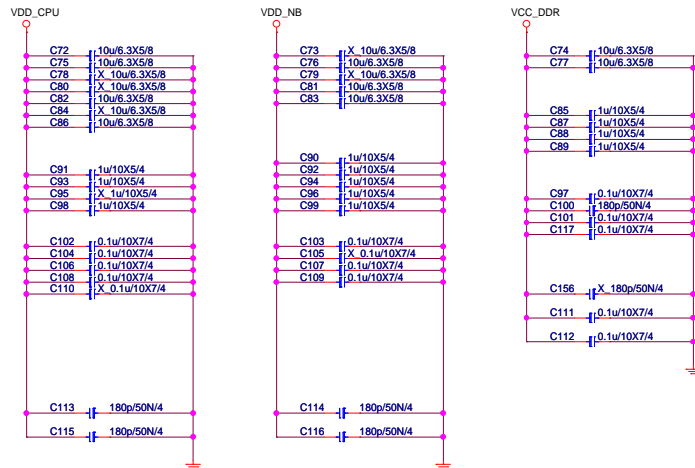
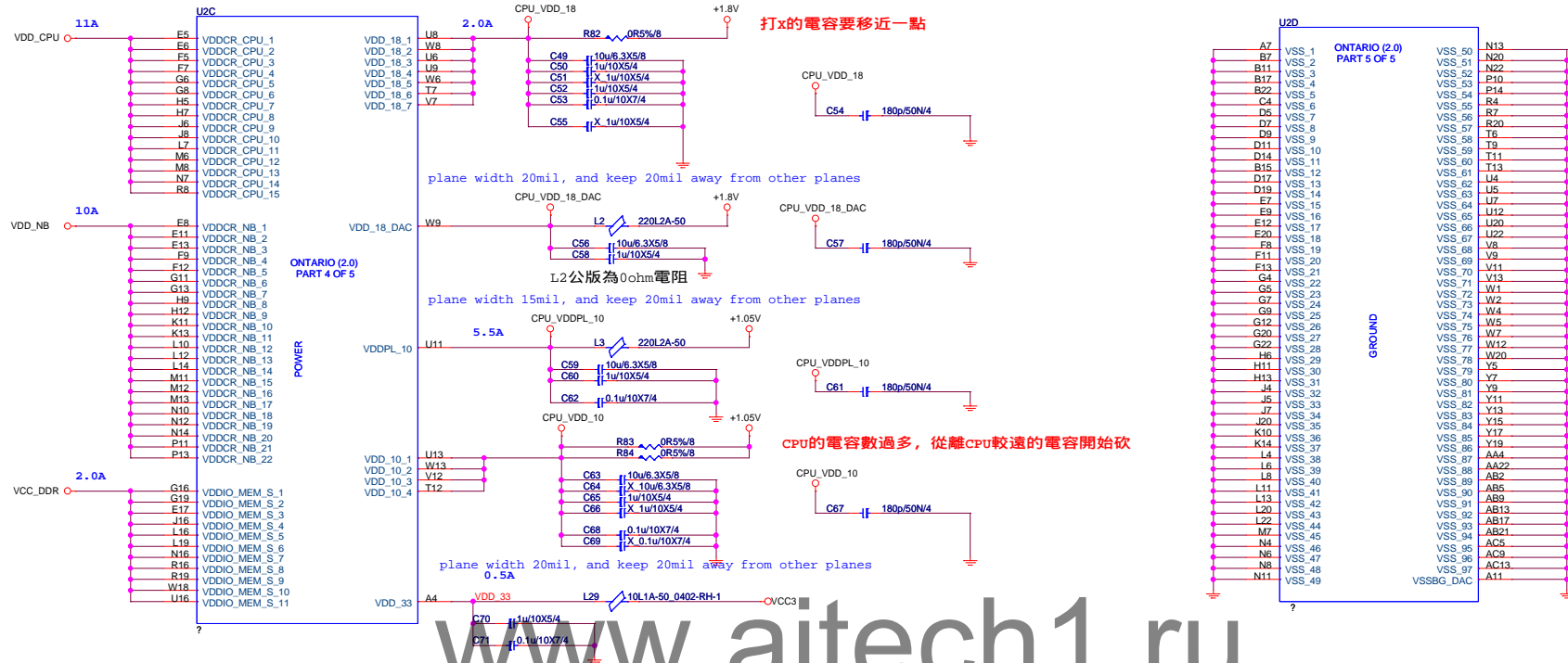


APU		MSI	OA0-1245002	.CPU_E350 DUAL CORE,AMD/ZM161032B2238,1.6GHz,BGA-413pin,REV.A1 18W ENGINEERING SAMPLE,RoHS COMPLIANCE
CPU		MSI	OA0-1245003	.CPU_E240 SINGLE CORE,AMD/ZM151032B1238,1.5GHz,BGA-413pin,REV.A1 18W 512K ENGINEERING SAMPLE,RoHS COMPLIANCE

目前上的料號是OA0-1245002 !!
 ECRECN要申請兩份BOM 只有CPU料號不同其餘皆同



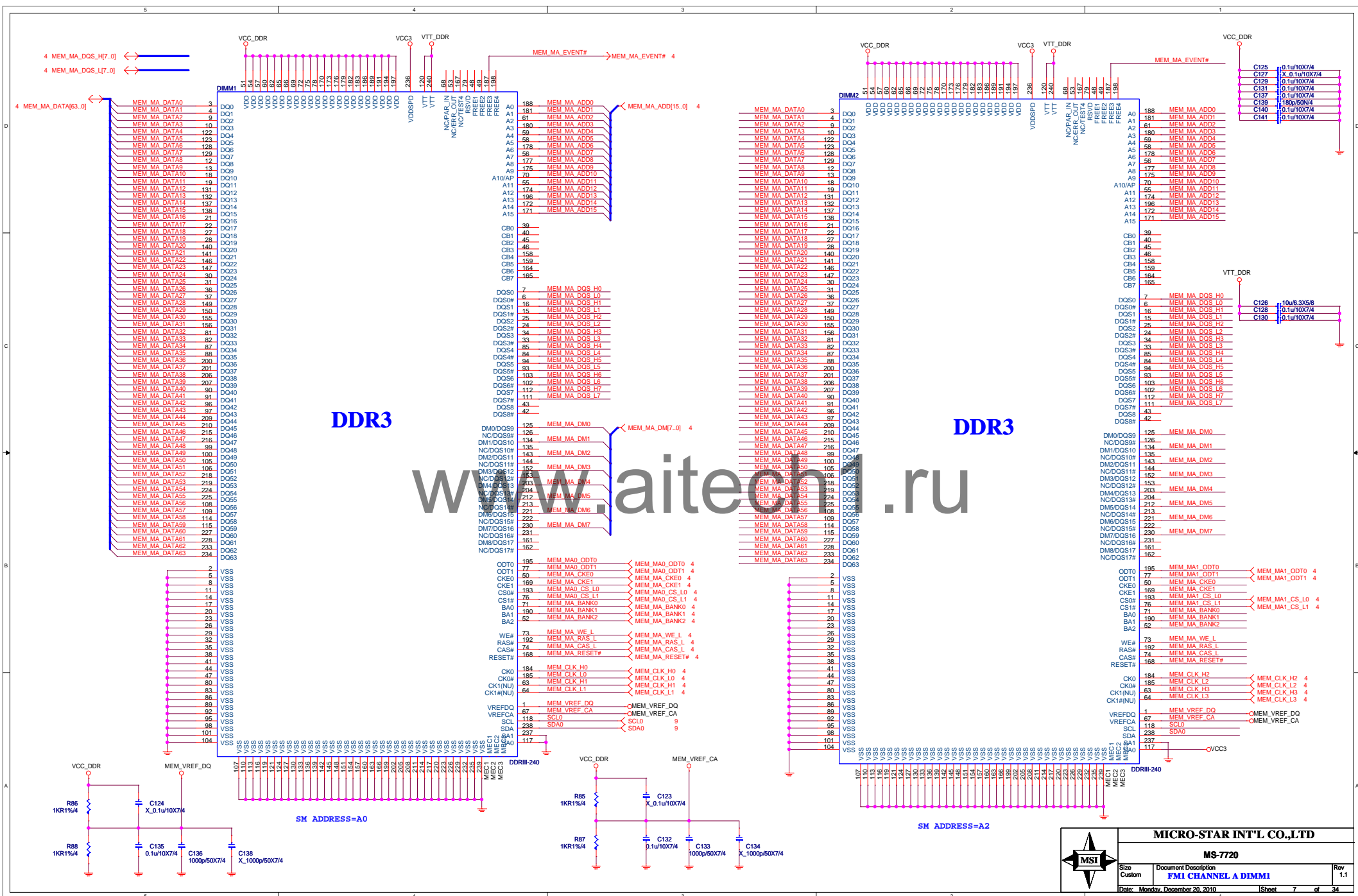
CPU AM3 PWR & GND

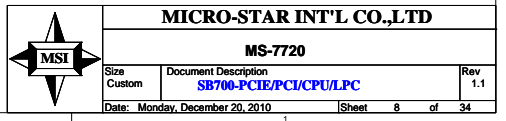


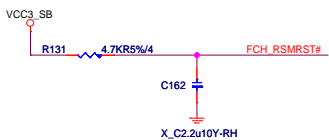
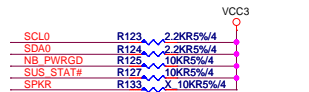
MICRO-STAR INT'L CO.,LTD

MS-7720

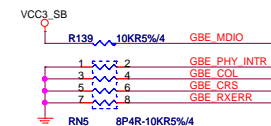
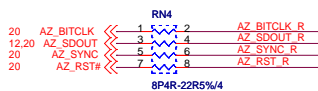
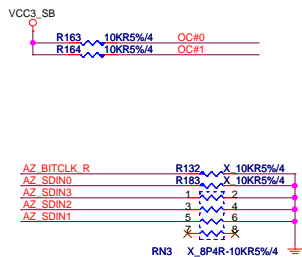
Size	Document Description	Rev
Custom	CPUFMI PWR&GND	1.1
Date: Monday, December 20, 2010	Sheet 6 of 34	







公板使用RC delay, 所以預留R130可以斷開從SIO來的RSMRST#, 另外公版是使用3.3Vdual pull high

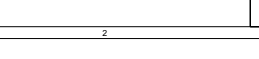
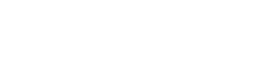
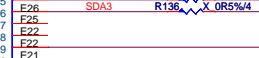
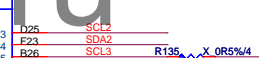
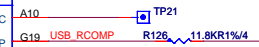
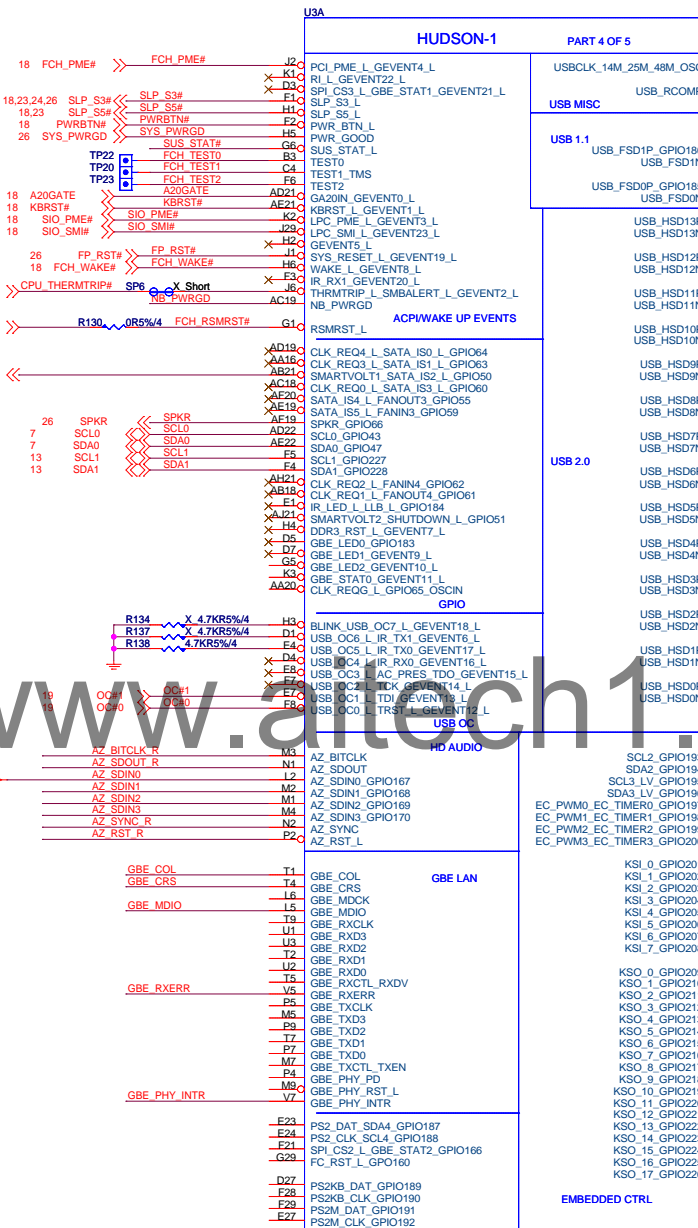


Grouping:

- SCL0, SDA0 (Primary SMBUS in the S0 domain)
- SCL1, SDA1 (Secondary SMBUS supporting ASF)
- SCL2, SDA2 (Primary SMBUS in the S5 domain)
- SCL3, SDA3 (Primary low-voltage SBMBUS for Processor TSI)
- SCL4, SDA4 (Primary SMBUS in the S5 domain)

Confirm FCH internal pull-up resistor to VDDIO_33_S is disable to prevent leakage when APU is powered down

20

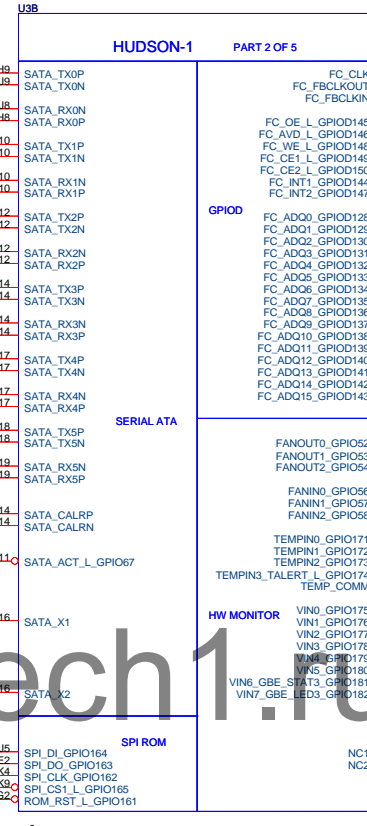
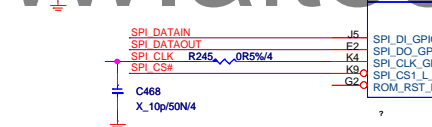
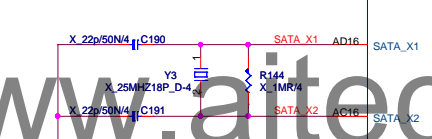
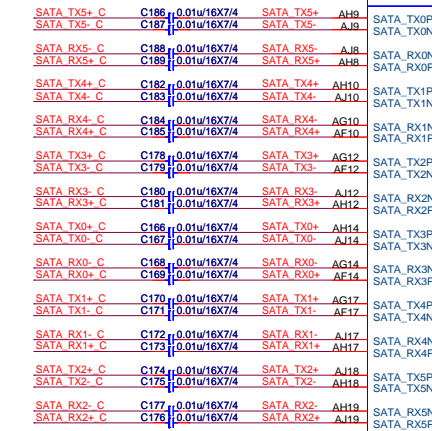
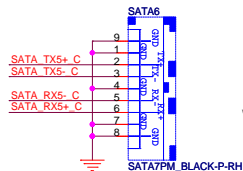
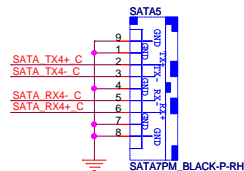
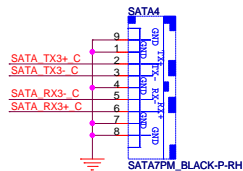
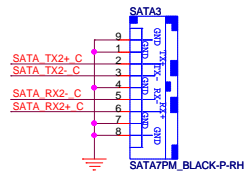
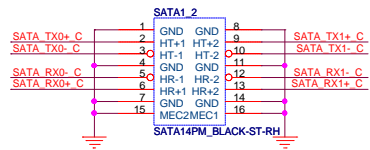


MICRO-STAR INT'L CO.,LTD

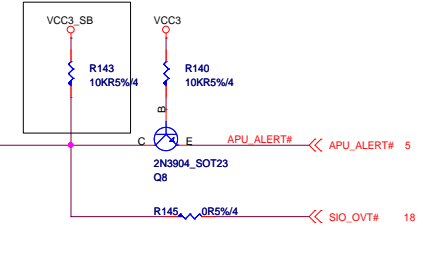
MS-7720

Size	Document Description	Rev
Custom	SB700-ACPI/GPIO/USB/AUDIO	1.1

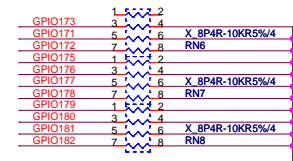
Date: Monday, December 20, 2010 Sheet 9 of 34



公板沒有pull high, 但是datasheet沒有內部pull high

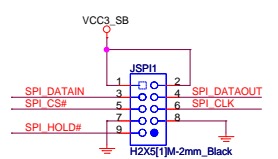


BIOS po 成output, 回來測試ok後拔掉!



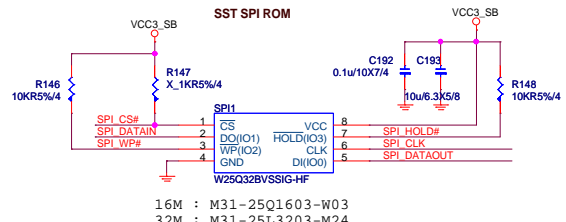
SPI DEBUG PORT

Place close to SPI ROM

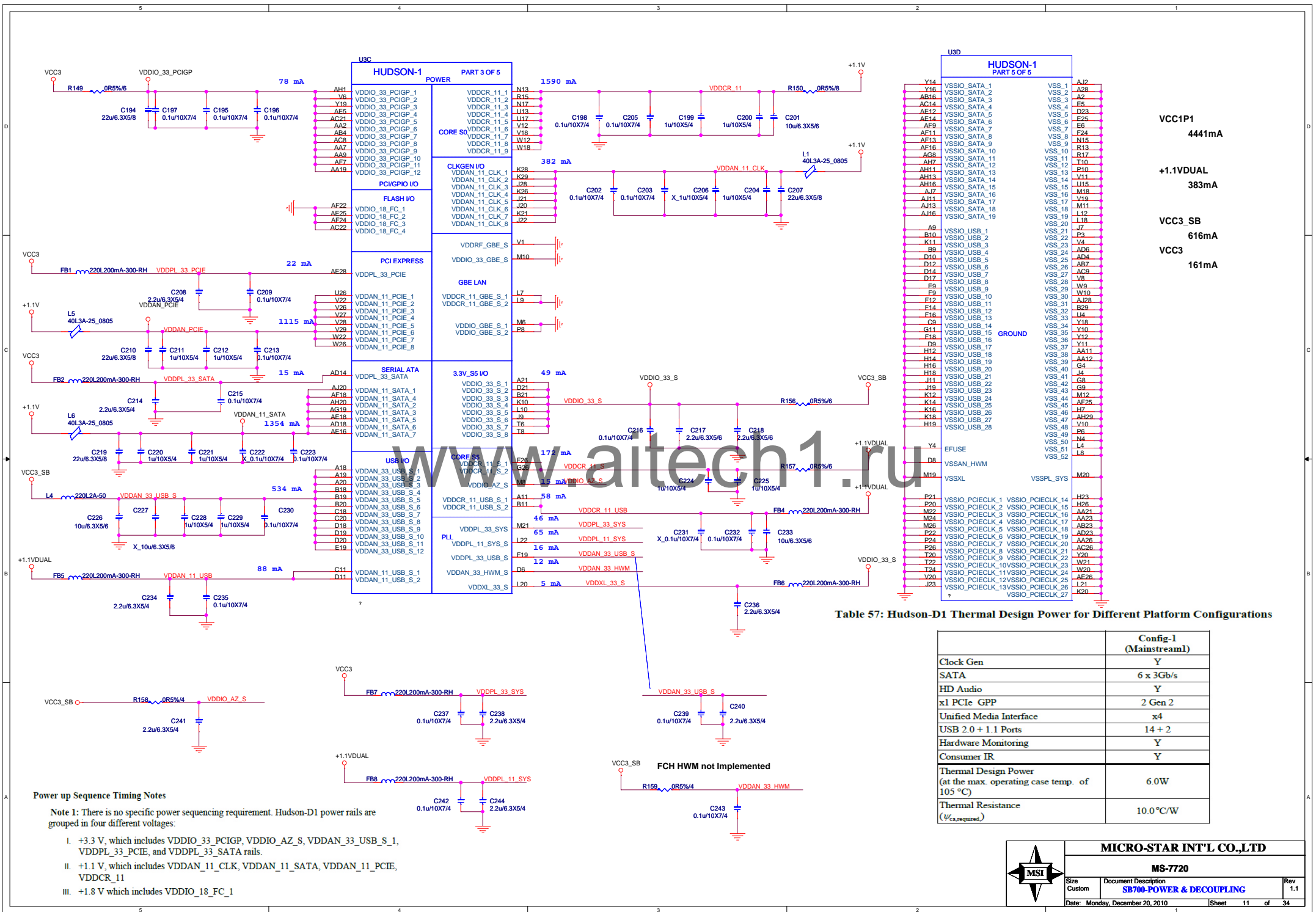


SPI 4/32M FLASH ROM

內部有pull high, 但是公板有R147上件

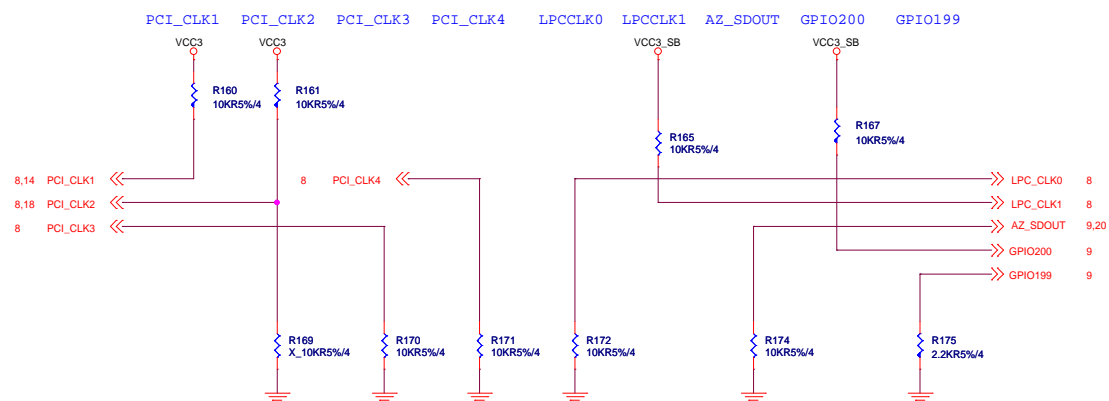


16M : M31-25Q1603-W03
32M : M31-25L3203-M24



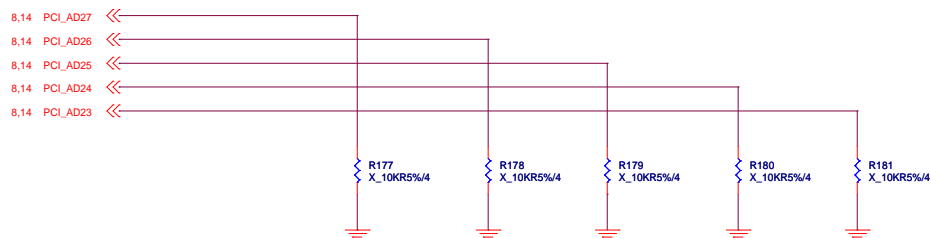


REQUIRED STRAPS



	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	AZ_SDOUT	GPIO200	GPIO199
PULL HIGH	PCIE GEN2 DEFAULT	WatchDog Enable DEFAULT	Debug Straps Enable	NON-Fusion APU clock mode	EC ENABLE	Internal clock mode DEFAULT	Reserved (as low power mode is not supported)	1	0
PULL LOW	PCIE GEN1	WatchDog Disable	Debug Straps Disable DEFAULT	Fusion APU clock mode DEFAULT	EC DISABLE DEFAULT	External clock mode DEFAULT	Required settling (performance mode) DEFAULT		SPI ROM

INTERNAL Pull-Up FOR PCI_AD[23/24/26/27]



FCH DEBUG STRAPS

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	ILA AUTORUN DISABLE DEFAULT	Use internal PLL FC Clk DEFAULT	Disable I2C ROM DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ILA AUTORUN ENABLE	Bypass internal FC Clk	Getting the value from I2C EPROM	ENABLE PCI MEM BOOT

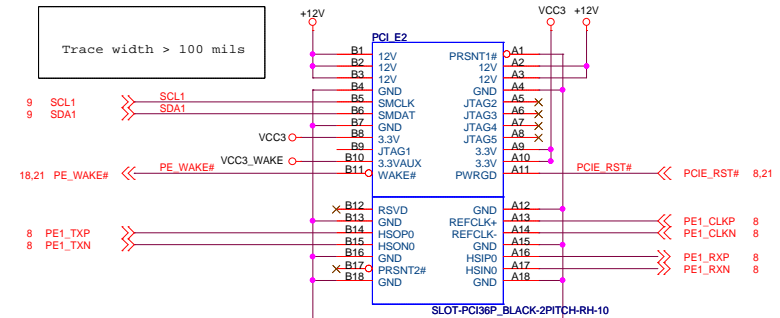
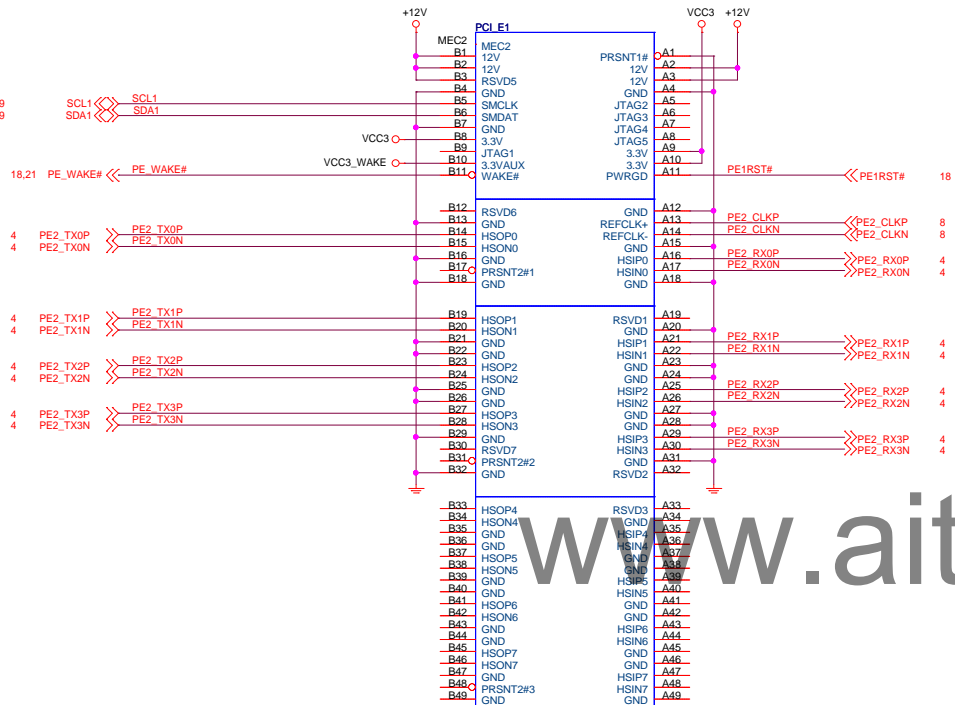


MICRO-STAR INT'L CO.,LTD

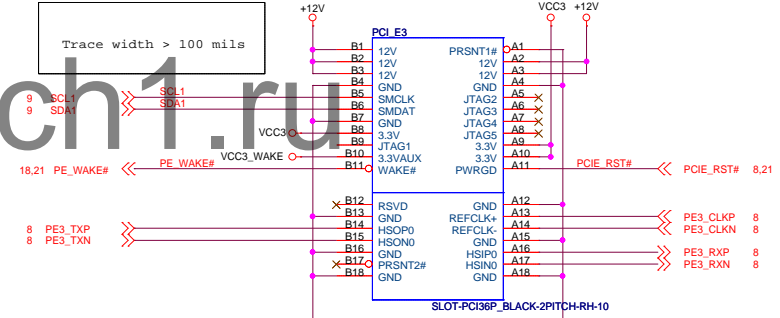
MS-7720

Size Custom	Document Description SB700-STRAPS	Rev 1.1
Date: Monday, December 20, 2010	Sheet 12 of 34	

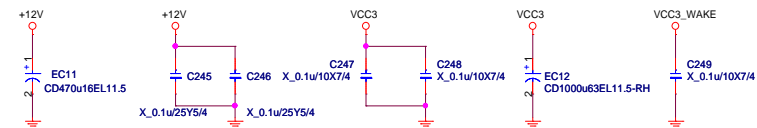
PCI EXPRESS x16 Slot



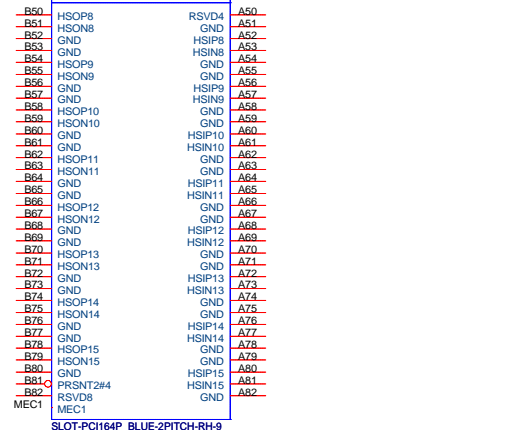
N11-0360281-K06



N11-0360281-K07

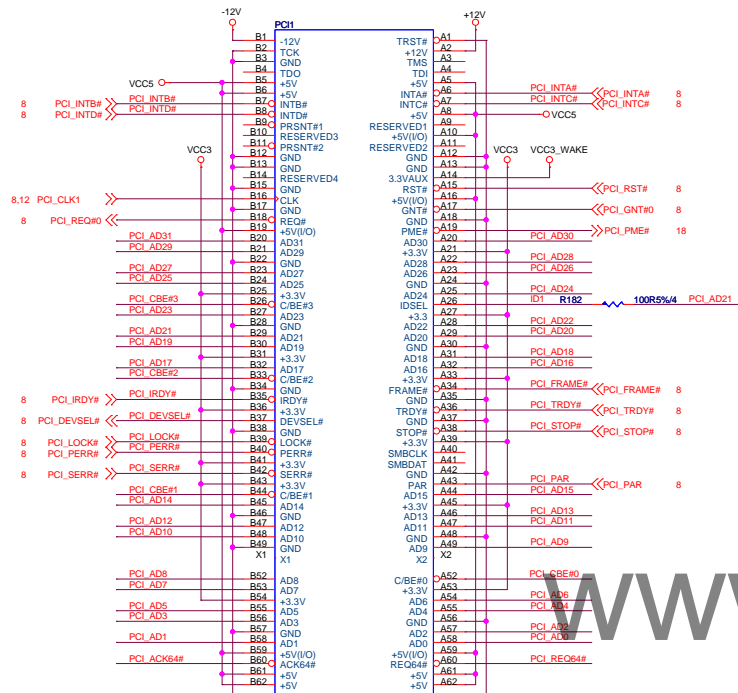


PCI Express X4 slot(X1)	
+12V	- 2.2 A
+3.3Vaux (wake)	- 375mA
+3.3Vaux (no wake)	- 20mA
+3.3V	- 3.0A
PCI Express X1 slot (X2)	
+12V	- 1 A
+3.3Vaux (wake)	- 750mA
+3.3Vaux (no wake)	- 40mA
+3.3V	- 6.0A



8,12 PCI_AD[31..0] << PCI_AD[31..0]
8 PCI_CBE[3..0] << PCI_CBE[3..0]

PCI SLOT 1 (PCI VER: 2.2 COMPLY)

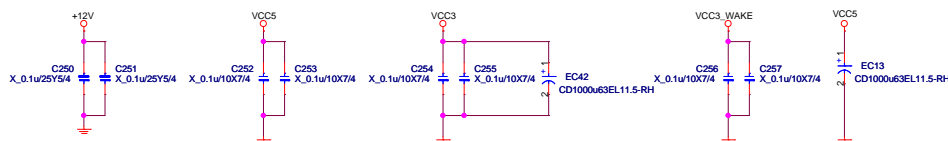


SLOT-PCI120P_BLACK-RH
N11-1200391-F02 (Black)

IDSEL = AD21
MASTER = PCI_REQ#0
PCI_GNT#0

PCI slot (X1)

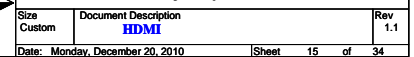
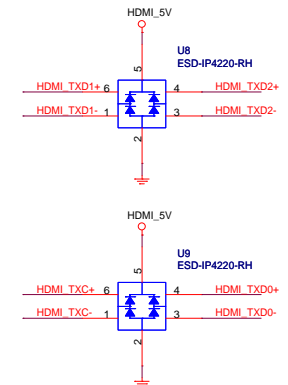
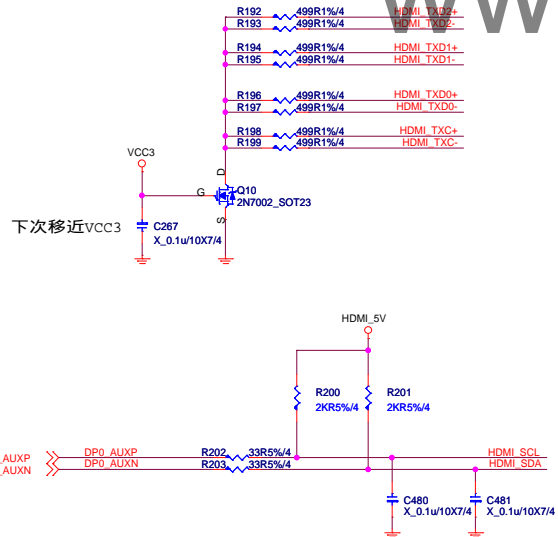
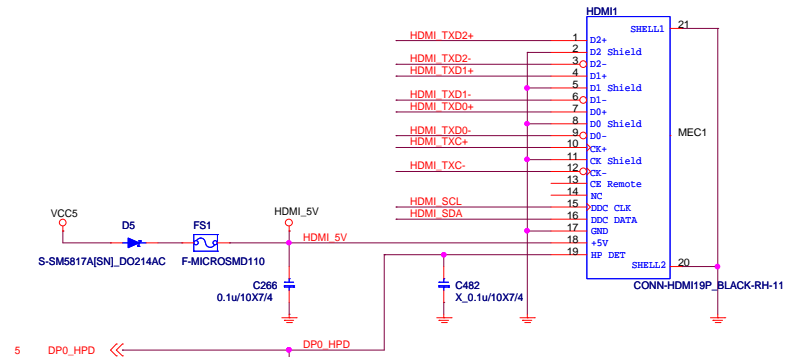
+3.3Vaux (wake)	- 375mA
+3.3Vaux (no wake)	- 20mA
+3.3V	- 7.6A
+5V	- 5A
+12V	- 0.5A

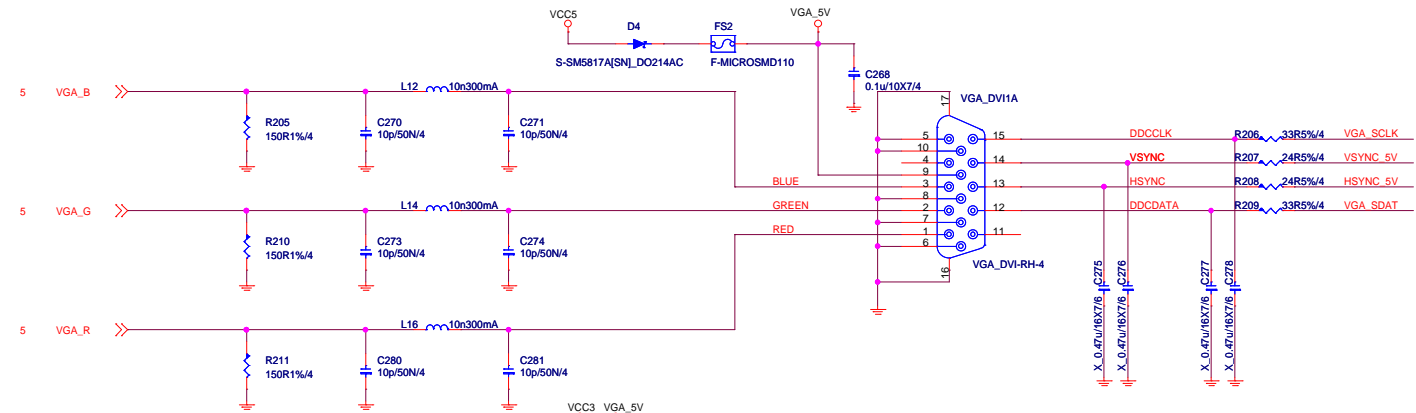


MICRO-STAR INT'L CO.,LTD

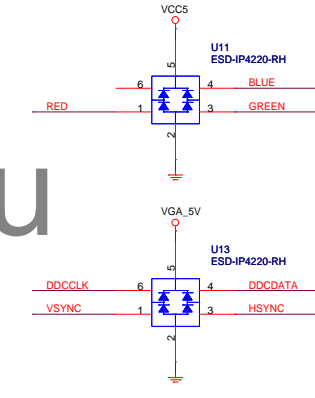
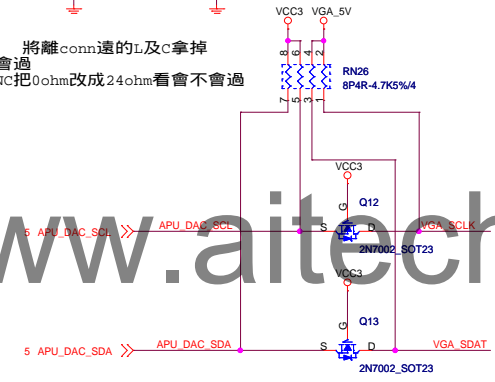
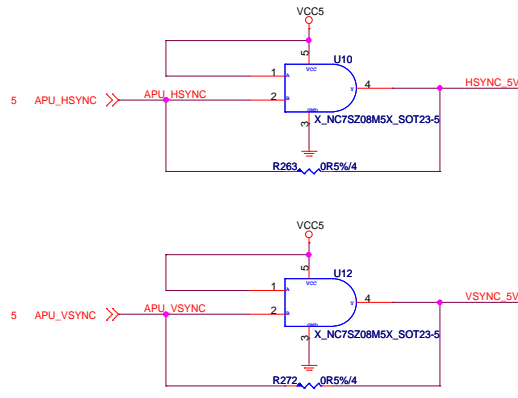
MS-7720

Size	Document Description	Rev
Custom	PCI X2	1.1
Date: Monday, December 20, 2010 Sheet 14 of 34		

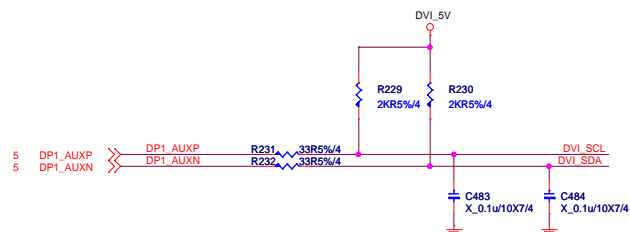
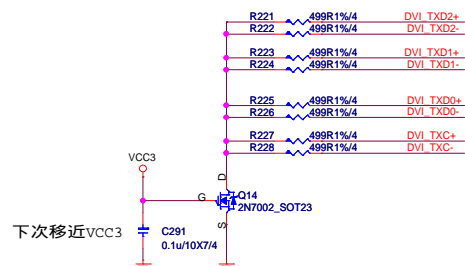
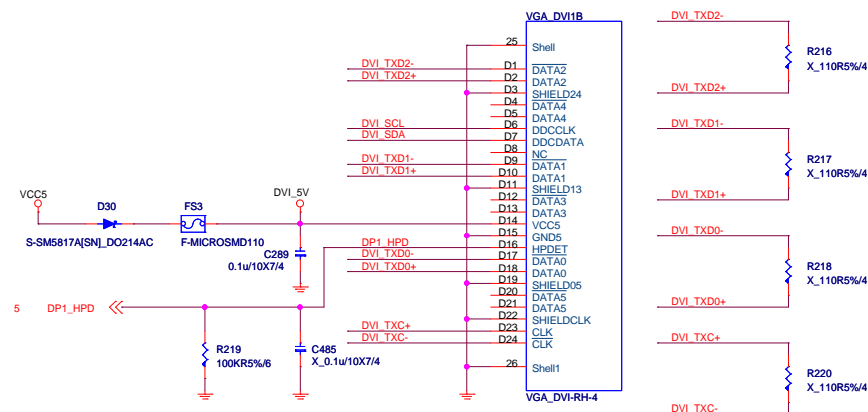
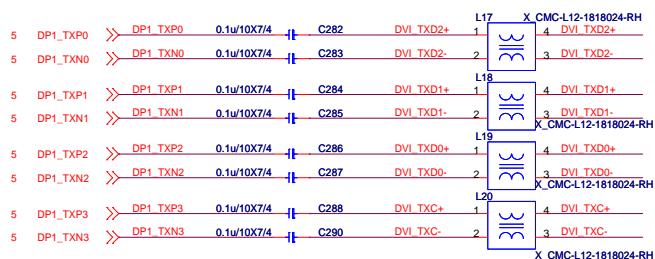




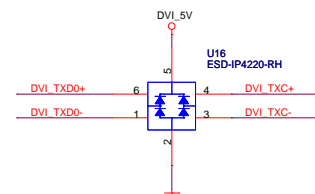
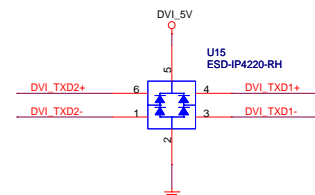
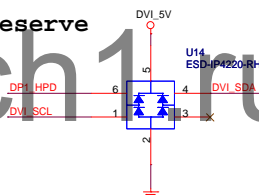
1. 雙pi型電路 將離conn遠的L及C拿掉
再看會不會過
2. HSYNC與VSYNC把0ohm改成24ohm看會不會過



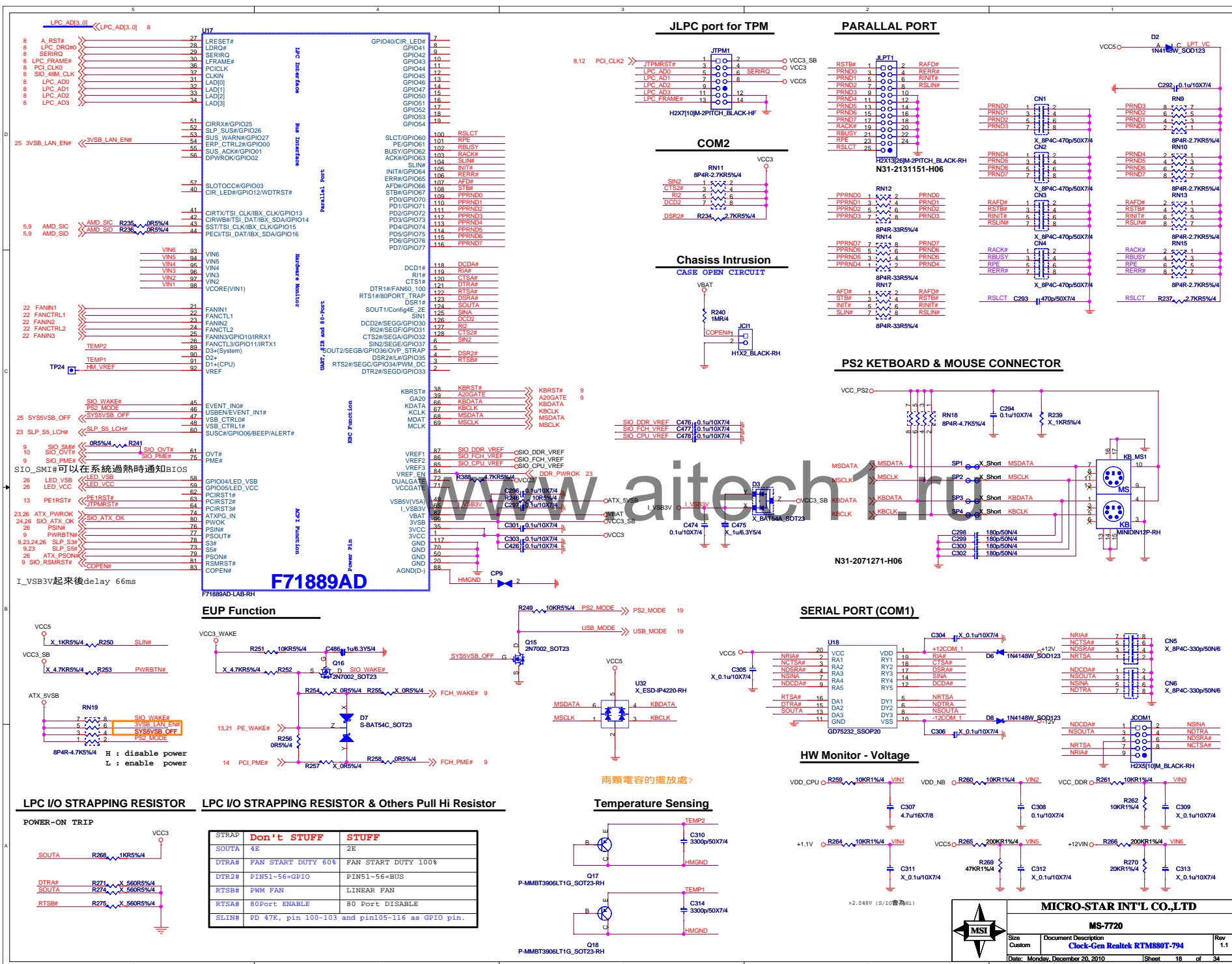
www.aitech1.ru

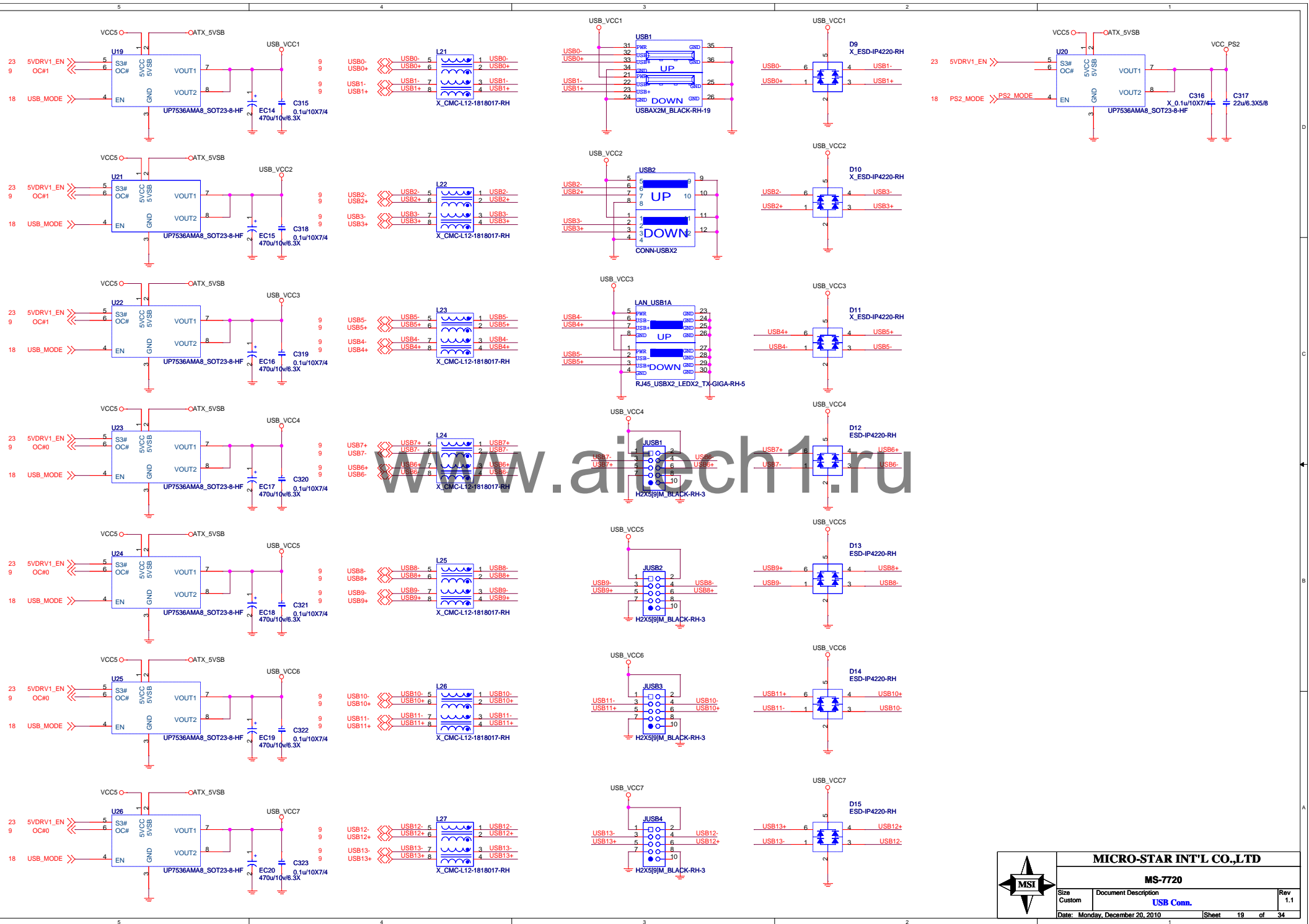


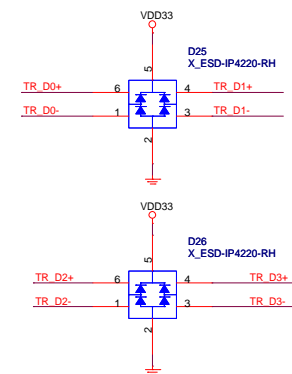
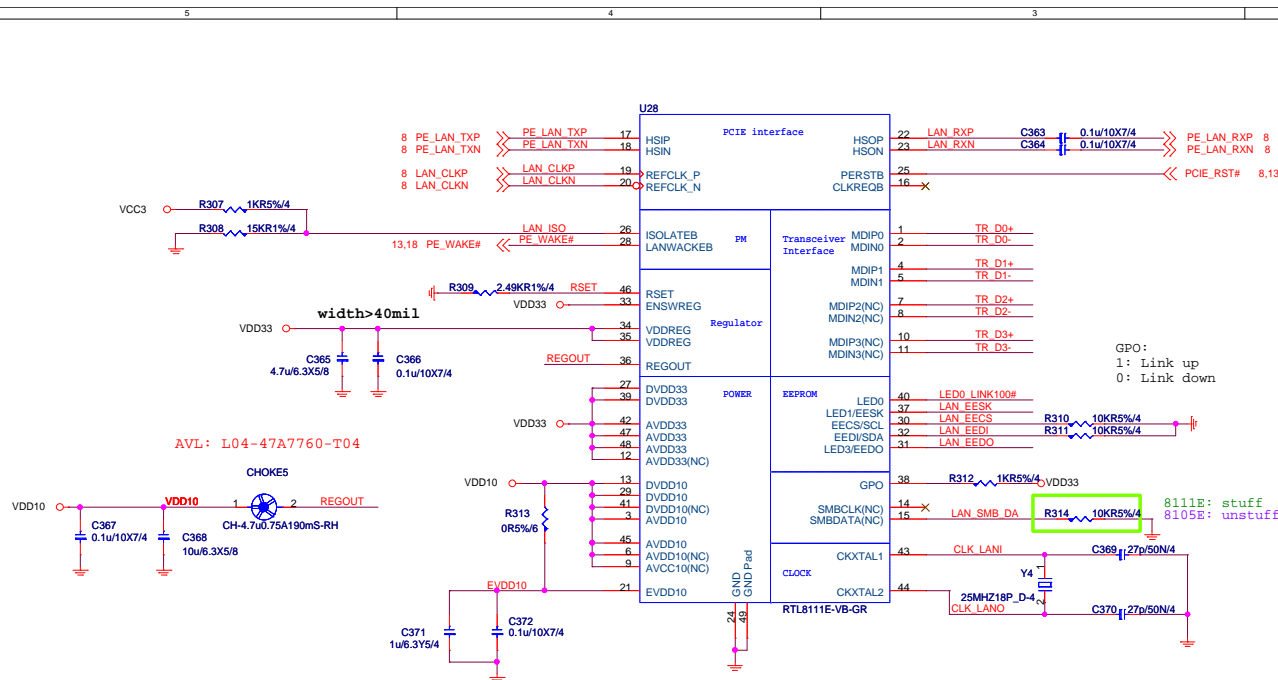
reserve



www.aitech1.ru



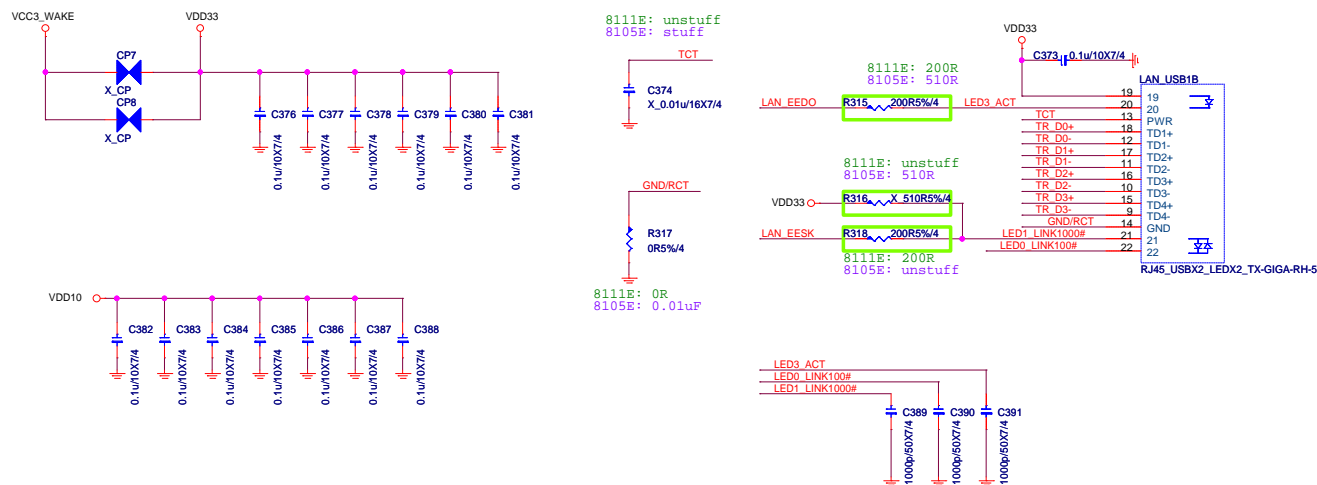




2pF D0G-0200529-A68 D0G-0303309-C12
1pF D0G-0422003-P03 D0G-0422003-N47

LAN			
+3.3V	VDD33	-	70mA
+1.05V	VDD10	-	300mA

www.aitech1.ru

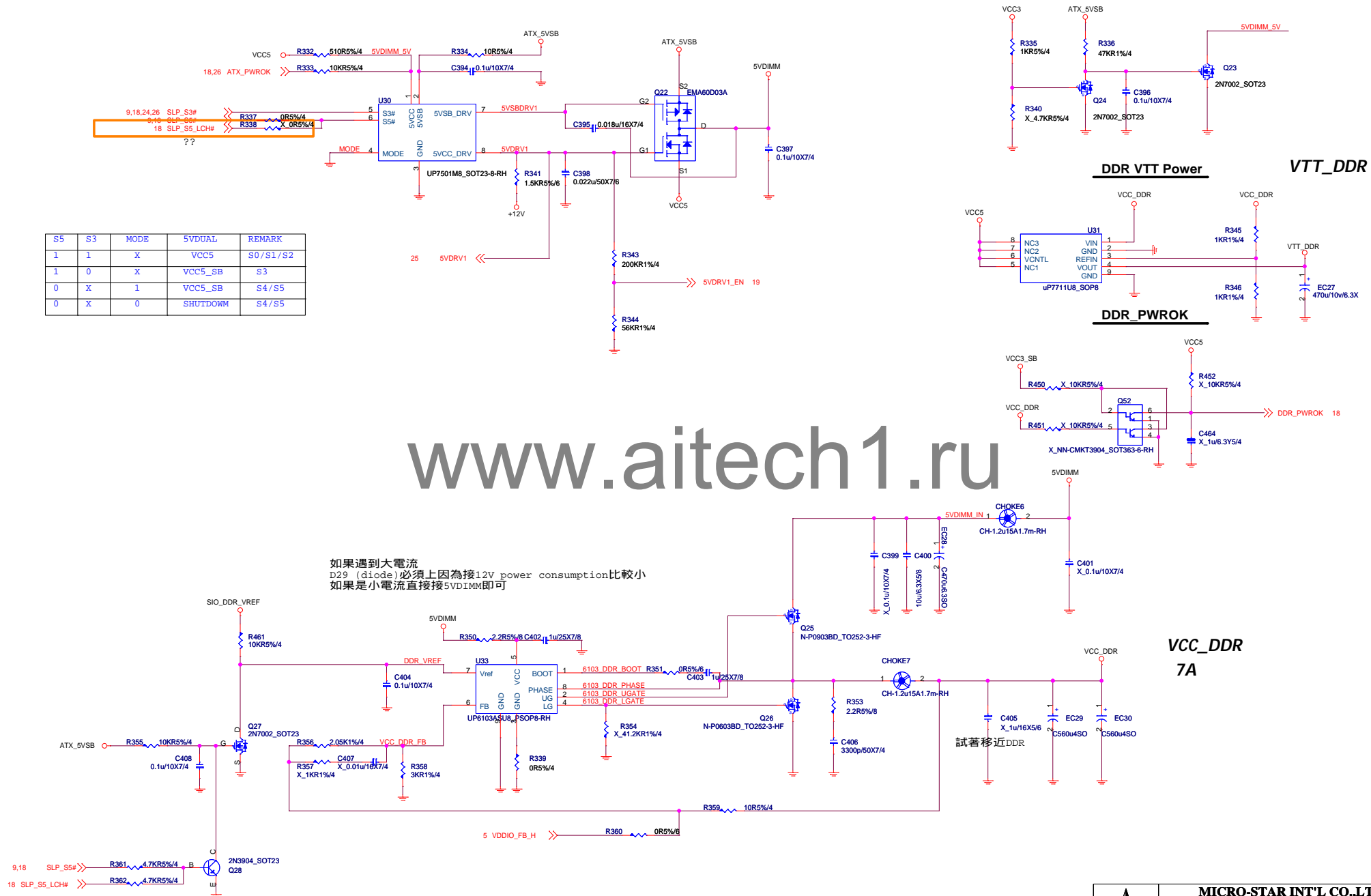


Giga-Lan	10/100-Lan
N58-22F0731 Link Yellow Active Blinking 1000 Orange 100 Green 10 None	N58-22F0771 Link Yellow Active Blinking 100 Green 10 None
19 20 21 22	19 20 21 22

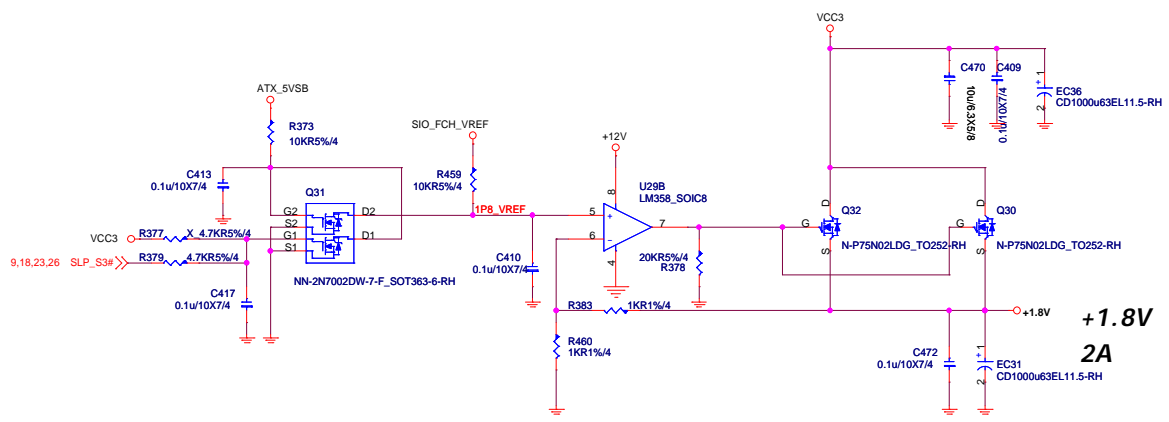
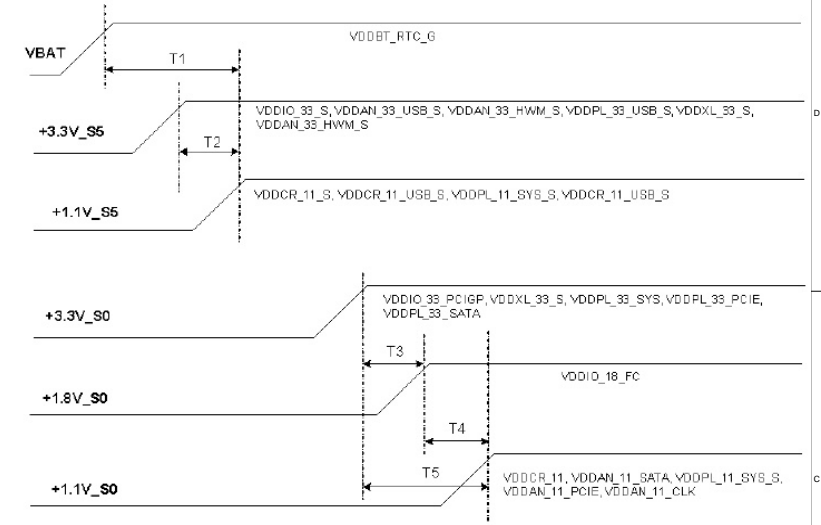
S5	S3	MODE	5VDUAL	REMARK
1	1	X	VCC5	S0/S1/S2
1	0	X	VCC5_SB	S3
0	X	1	VCC5_SB	S4/S5
0	X	0	SHUTDOWN	S4/S5

www.aitech1.ru

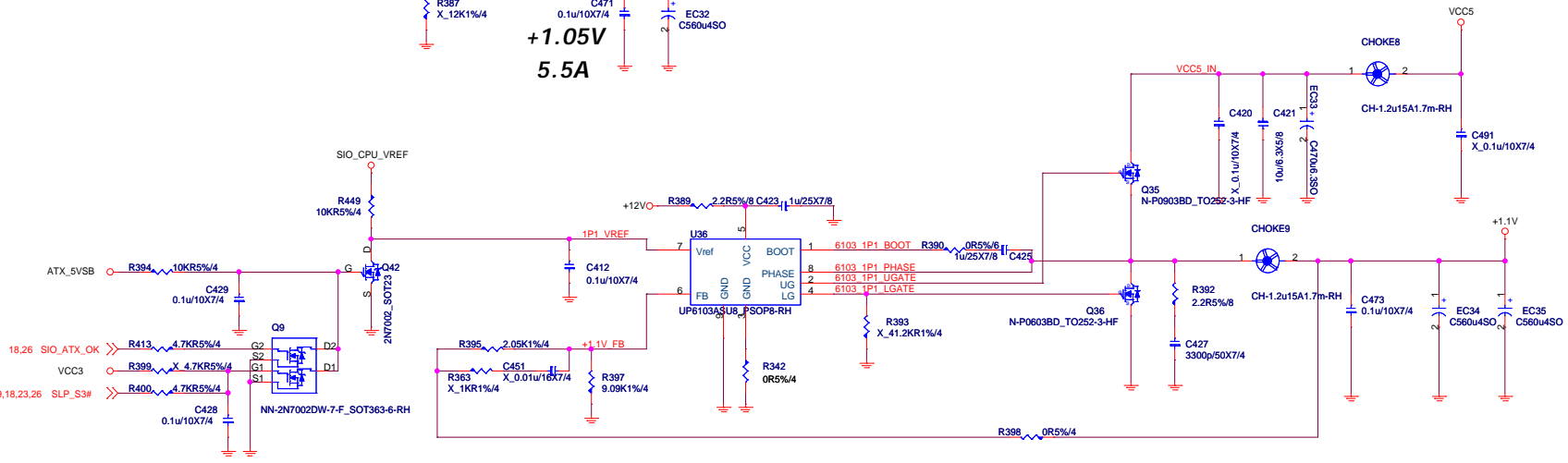
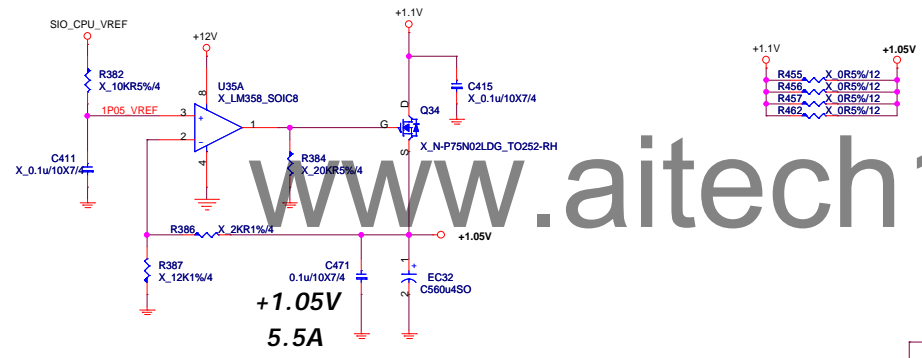
如果遇到大電流
D29 (diode) 必須上因為接12V power consumption比較小
如果是小電流直接接5VDIMM即可

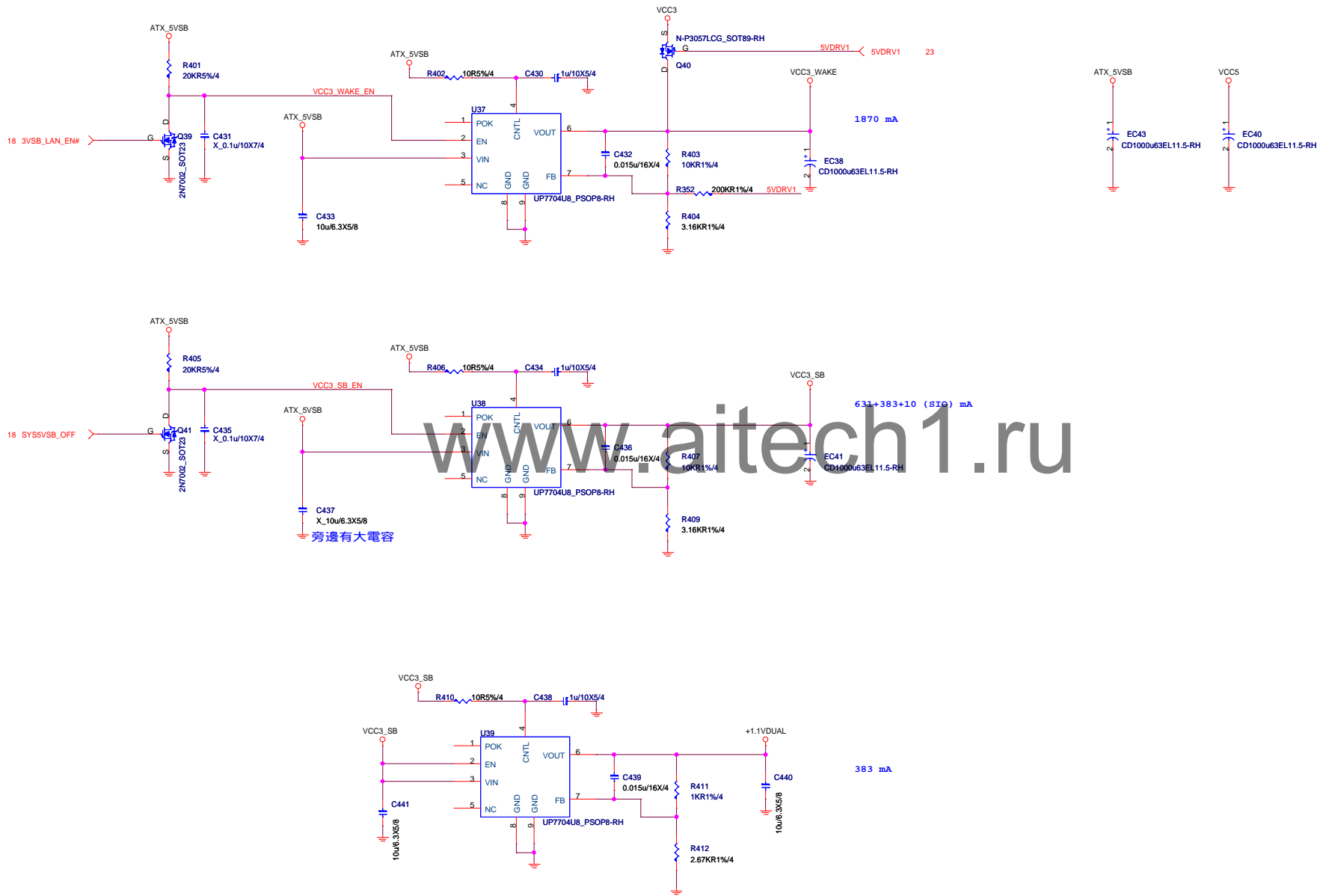


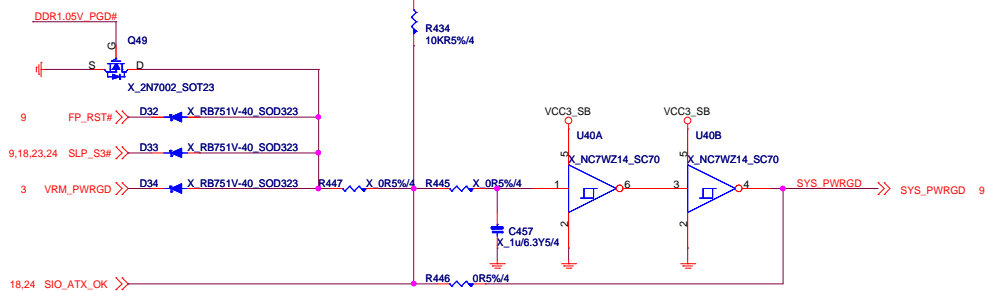
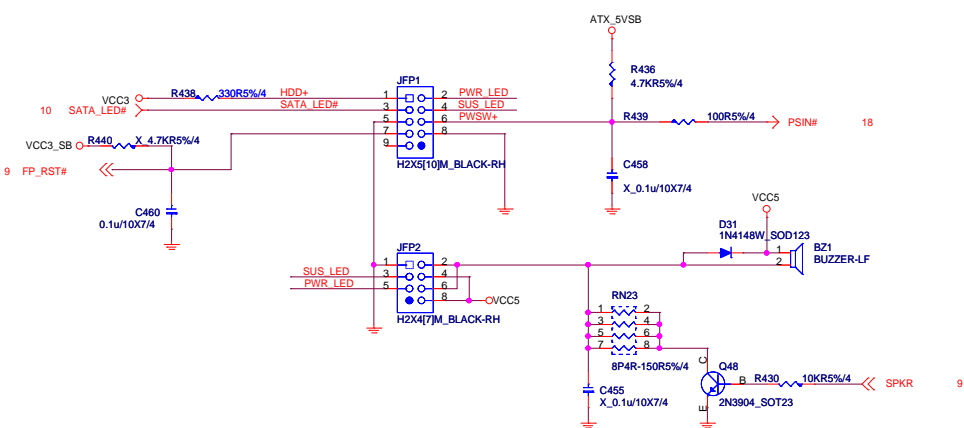
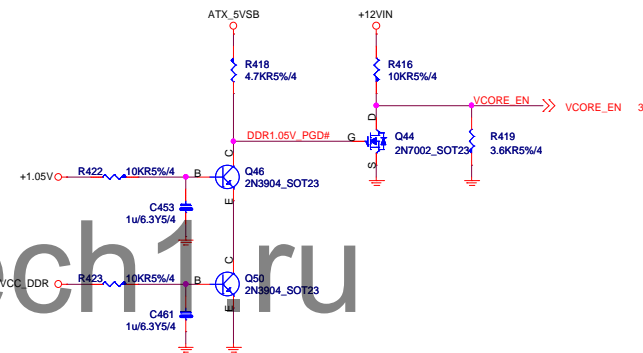
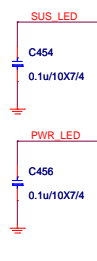
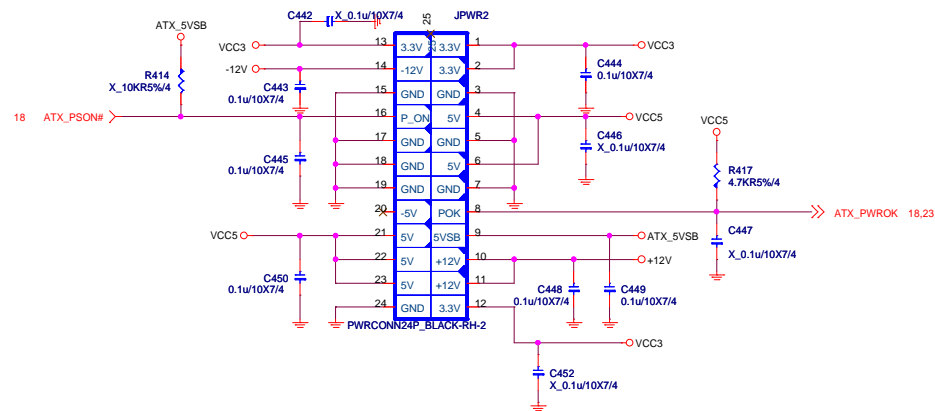
The Hudson-1 power rail power-up sequence is shown below. In general, the requirement is that lower voltages must never exceed higher voltages during power up.



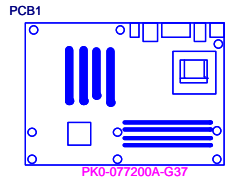
注意1.05V與1.1V的拉載視情況要再補一些電容





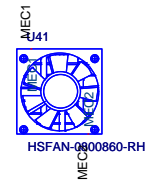
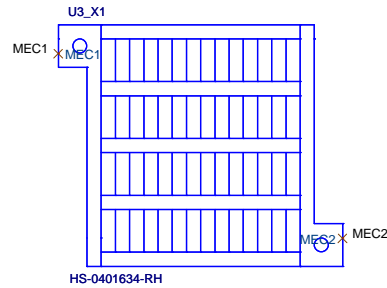
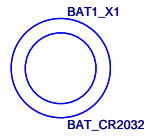


PCB

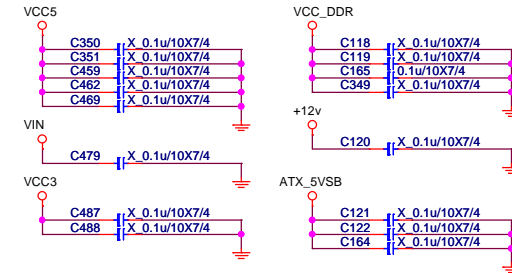


PCB : 1080
PK0-0772011-E36

BATTERY



FOR EMI



E350M-E33

LABEL1

LABEL

X_AMI-BIOS-LABEL

BUMPER1

BUMPER

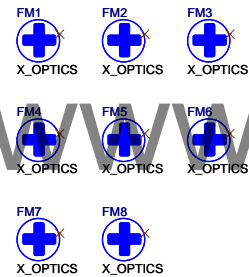
X_BUMPER

BUMPER2

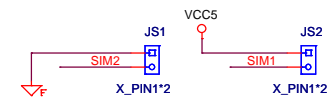
BUMPER

X_BUMPER

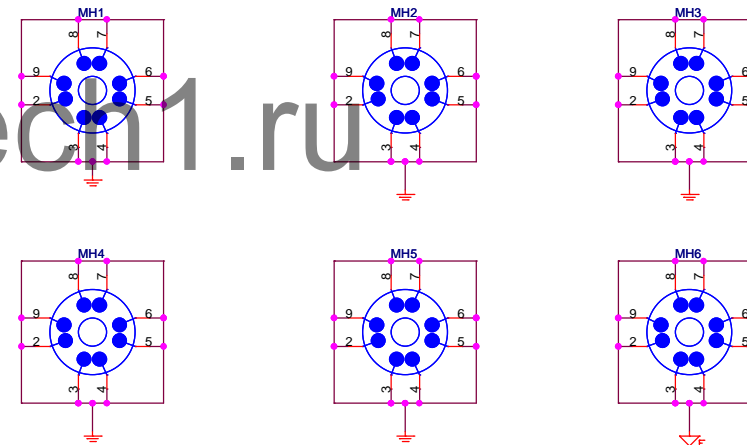
Optics Orientation Holes



Simulation



Mounting Holes



MICRO-STAR INT'L CO.,LTD

MS-7720

Size	Document Description	Rev
Custom	BOM - Option Parts	1.1
Date: Monday, December 20, 2010	Sheet 27 of 34	